

FIG. 1
Prior Art

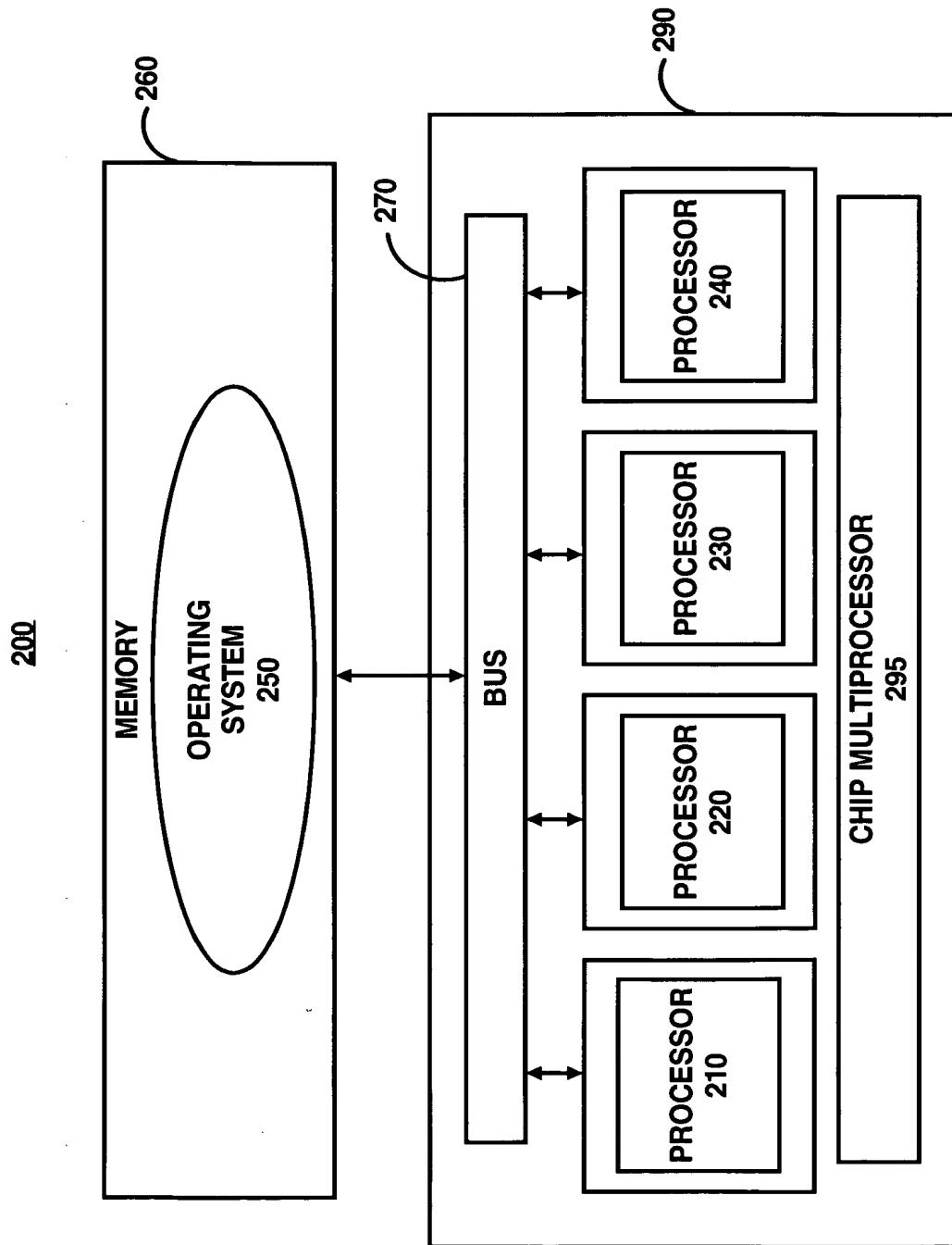


FIG. 2
Prior Art

CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

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3/4

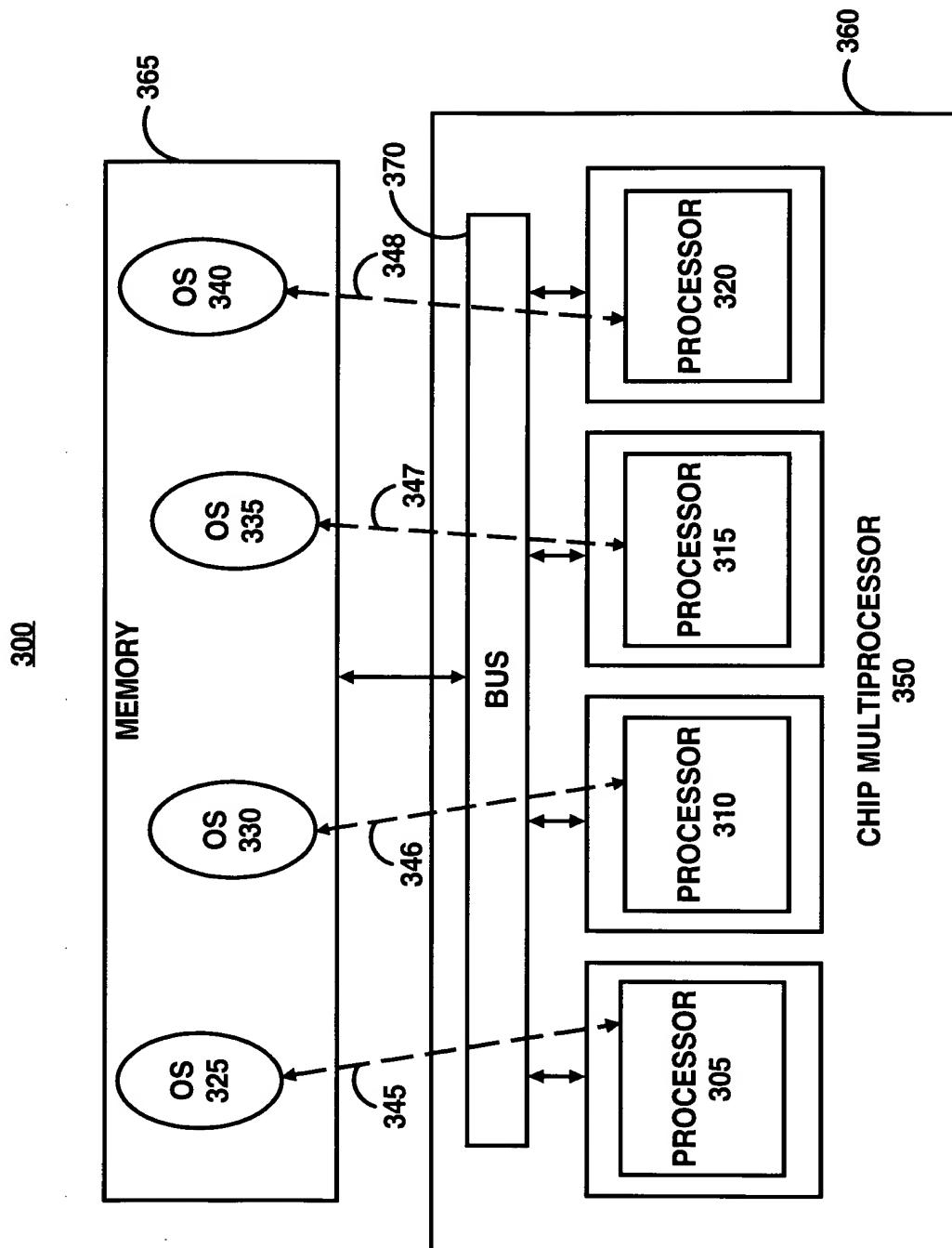


FIG. 3

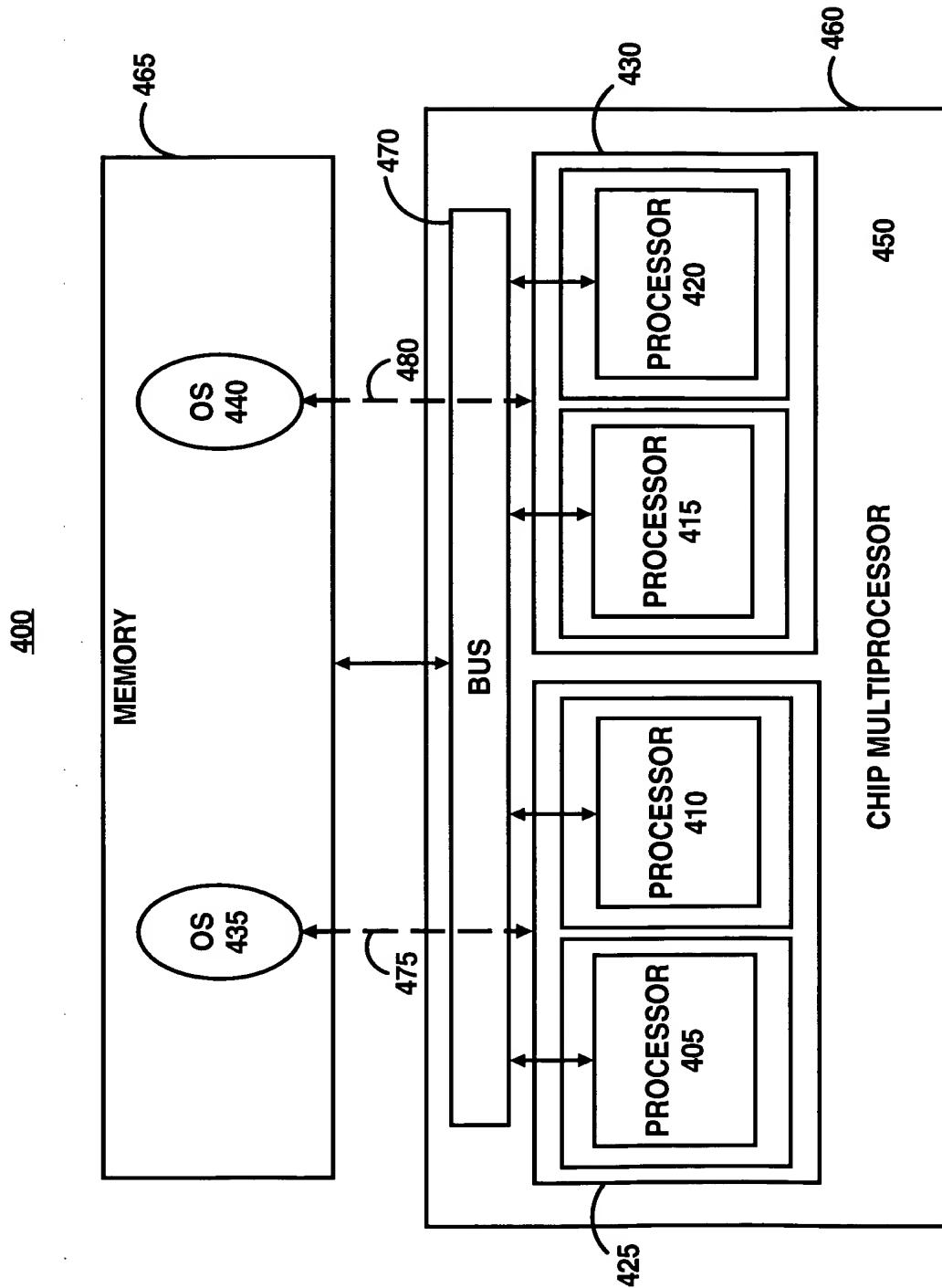


FIG. 4